IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

JOHANN FUHRMANN ET AL | DE 010007

Serial No.

Filed: CONCURRENTLY

ELECTRIC OR ELECTRONIC CIRCUIT ARRANGEMENT AND METHOD OF PROTECTING SAID CIRCUIT ARRANGEMENT FROM MANIPULATION AND/OR ABUSE

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. A circuit arrangement (100) as claimed in claim 1, characterized in that the mutual distance (d) between the conductor tracks (20, 25) is in the micrometer range.

4. A circuit arrangement (100) as claimed in claim 1, characterized in that the material of the dielectric shielding layer (30; 35) is epoxy resin or silicon nitrite ($SiNO_2$) or silicon dioxide (SiO_2) or consists of other insulating layers used in the manufacture of semiconductors.

5. A circuit arrangement (100) as claimed in claim 1, characterized in that the material of the dielectric shielding layer (30; 35) is also opaque.

6. A circuit arrangement (100) as claimed in claim 1, characterized in that the signal-generating unit (40) comprises at least one oscillator circuit consisting of at least one capacitive unit, particularly a capacitor, and at least one resistive unit, particularly a resistor, and/or at least one oscillator circuit consisting of at least one capacitive unit, particularly a capacitor, and at least one inductive unit, particularly a coil.

7. A circuit arrangement (100) as claimed in claim 1, characterized in that at least an evaluation unit (70), particularly at least a differential evaluation unit is constituted by the first counting unit (50), the second counting unit (55) and the comparator unit (60).

9. A circuit arrangement (100) ad claimed in claim 7, characterized in that the evaluation unit (70) generates the error indication when the actual value deviates from the nominal range.

10. A circuit arrangement (100) as claimed in claim 1, characterized in that the first counting unit (50) and/or the second counting unit (55) is formed on a digital basis.

11. A card, particularly a chip card or smart card, comprising at least an electric or electronic circuit arrangement (100) as claimed in claim 1.

15. A method as claimed in claim 13, characterized in that the error indication is generated in the evaluation unit (70) when the actual value deviates from the nominal range.

REMARKS

The foregoing amendments to claims 3-7, were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore reserves his right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By__________________________
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APPENDIX

3. A circuit arrangement (100) as claimed in claim 1 ~~or 2~~, characterized in that the mutual distance (d) between the conductor tracks (20, 25) is in the micrometer range.

4. A circuit arrangement (100) as claimed in claim 1~~any one of claims 1 to 3~~, characterized in that the material of the dielectric shielding layer (30; 35) is epoxy resin or silicon nitrite ($SiNO_2$) or silicon dioxide (SiO_2) or consists of other insulating layers used in the manufacture of semiconductors.

5. A circuit arrangement (100) as claimed in claim 1~~any one of claims 1 to 4~~, characterized in that the material of the dielectric shielding layer (30; 35) is also opaque.

6. A circuit arrangement (100) as claimed in claim 1~~any one of claims 1 to 5~~, characterized in that the signal-generating unit (40) comprises at least one oscillator circuit consisting of at least one capacitive unit, particularly a capacitor, and at least one resistive unit, particularly a resistor, and/or at least one oscillator circuit consisting of at least one capacitive unit, particularly a capacitor, and at least one inductive unit, particularly a coil.

7. A circuit arrangement (100) as claimed in claim 1~~any one of claims 1 to 6~~, characterized in that at least an evaluation unit (70), particularly at least a differential evaluation unit is constituted by the first counting unit (50), the second counting unit (55) and the comparator unit (60).

9. A circuit arrangement (100) ad claimed in claim 7 ~~or 8~~, characterized in that the evaluation unit (70) generates the error indication when the actual value deviates from the nominal range.

10. A circuit arrangement (100) as claimed in claim 1~~any one of claims 1 to 9~~, characterized in that the first counting unit (50) and/or the second counting unit (55) is formed on a digital basis.

11. A card, particularly a chip card or smart card, comprising at least an electric or electronic circuit arrangement (100) as claimed in claim 1~~any one of claims 1 to 10~~.

15. A method as claimed in claim 13~~ or 14~~, characterized in that the error indication is generated in the evaluation unit (70) when the actual value deviates from the nominal range.